ABSTRACT

A semiconductor structure and method of processing same including a substrate, a lattice-mismatched first layer deposited on the substrate and annealed at a temperature greater than 100°C above the deposition temperature, and a second layer deposited on the first layer with a greater lattice mismatch to the substrate than the first semiconductor layer. In another embodiment there is provided a semiconductor graded composition layer structure on a semiconductor substrate and a method of processing same including a semiconductor substrate, a first semiconductor layer having a series of lattice-mismatched semiconductor layers deposited on the substrate and annealed at a temperature greater than 100°C above the deposition temperature, a second semiconductor layer deposited on the first semiconductor layer with a greater lattice mismatch to the substrate than the first semiconductor layer, and annealed at a temperature greater than 100°C above the deposition temperature of the second semiconductor layer.